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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 4 :		(11) International Publication Number:
G11C 5/00, G05F 5/00, 1/62	A1	WO 86/ 04724
		(43) International Publication Date: 14 August 1986 (14.08.86)

(21) International Application Number: PCT/US86/00160

(22) International Filing Date: 27 January 1986 (27.01.86)

(31) Priority Application Number: 699,794

(32) Priority Date: 8 February 1985 (08.02.85)

(33) Priority Country: US

(71) Applicant: AMERICAN TELEPHONE & TELEGRAPH COMPANY [US/US]; 550 Madison Avenue, New York, NY 10022 (US).

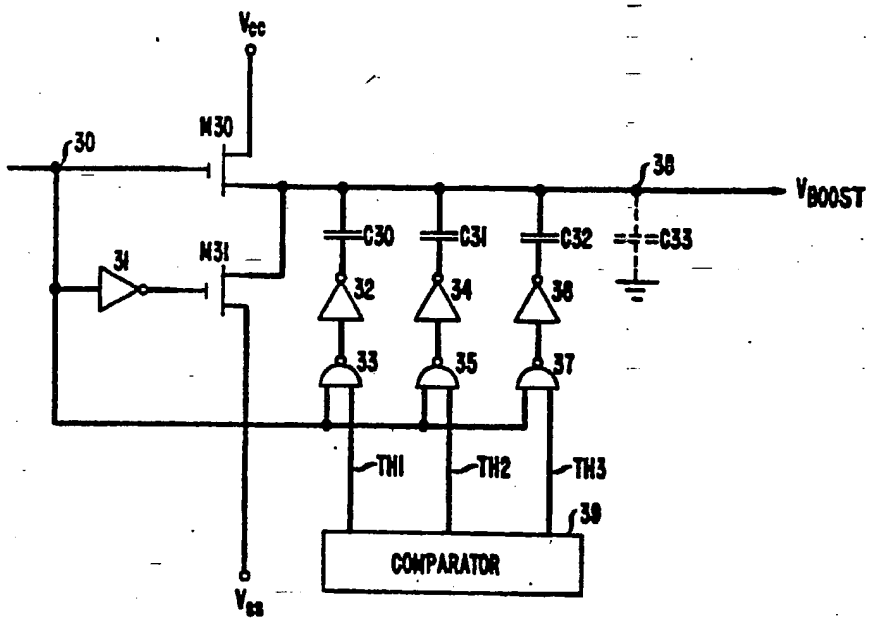
(72) Inventors: KIRSCH, Howard, Clayton ; Box 207A, RD #2, Oak Hill Road, Emmaus, PA 18049 (US). STEFANY, James, Harold ; RR2, Box 208, Asbury, NJ 08802 (US).

(74) Agents: HIRSCH, A., E., Jr. et al.; AT&T Bell Laboratories, Post Office Box 679, Holmdel, NJ 07733 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), FR (European patent), GB (European patent), IT (European patent), JP, KR, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: INTEGRATED CIRCUIT HAVING A VARIABLY BOOSTED NODE



(57) Abstract

An integrated circuit comprises a node (38) that is boosted by one or more boost capacitors depending on the level of the power supply voltage. When the level is below a given threshold, a first boost capacitor (30) is activated. Additional boost capacitors (C31, C33) may be provided for activation at still lower thresholds. The boost capacitors are deactivated when the power supply level exceeds the corresponding thresholds. In this manner, a more constant boosted voltage is obtained. This provides for an adequate boosted voltage at low power supply levels, while avoiding excessive boost at high power supply voltages that could damage devices. The technique may be used for boosted row conductors in dynamic random access memories, among other applications.

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INTEGRATED CIRCUIT HAVING A VARIABLY BOOSTED NODE

Background of the Invention

1. Field of the Invention

The present invention relates to an integrated circuit having at least one electrical conductor boosted to a voltage in excess of a power supply voltage.

2. Description of the Prior Art

The use of voltages in excess of the power supply voltage is common in integrated circuits, especially those implemented in field effect transistor (FET) technology. The "boosted node" technique is used typically to overcome the threshold voltage drop (Vth) of a FET when it is desired to pass a signal therethrough (i.e., from source to drain) without reducing the magnitude of the signal. For example, in dynamic random access memory (DRAM) design, the use of a boosted row conductor is typical. This technique increases the gate voltage on the access transistors in a selected row so that the threshold voltage drop does not substantially reduce the voltage level of the data stored in the respective storage capacitors.

One problem with prior art boost generators has become more apparent as the thickness of the gate oxides of devices connected to the boosted node are decreased. Then, the electric fields increase across such devices if the boost voltage is maintained at a given value. For example, the gate oxides of DRAM access transistors are subjected to excessive electrical stress if subjected to the high fields produced by prior art techniques over prolonged periods of time. This can lead to failure of a device, or degradation of its performance. Therefore, means have been included in boost generators to limit the amount of boost they produce. However, such means, in the past, have been found to excessively reduce the available boost voltage in situations where the supply voltage is somewhat low or to provide excessively high boost voltage when the supply voltage is relatively high.

Summary of the Invention

We have invented a boost generator circuit suitable for implementing in integrated circuit form wherein the degree of boost is varied by activating one or more boost capacitors. The number of capacitors providing the boost is determined by the level of the power supply voltage applied to the integrated circuit.

Brief Description of the Drawings

FIG. 1 illustrates an embodiment of the variable boost generator of the present invention.

FIG. 2 illustrates a circuit embodiment of a voltage comparator suitable for implementing the present invention.

FIG. 3 illustrates the boosted voltage versus power supply voltage for the circuit of FIG. 1.

Detailed Description

The following detailed description relates to a technique for varying the boost voltage on a boosted node. This technique provides for activating a varying number of boost capacitors depending upon the power supply voltage applied to an integrated circuit chip or wafer. This technique overcomes certain disadvantages of prior art diode limiting techniques. In particular, one prior art limiting technique provides that the boosted voltage increases linearly with power supply increases. Hence, at low Vcc values (e.g., 4.5 volts) the boosted voltage is relatively low (e.g., 5.1 volts). This can degrade the performance of circuits receiving the boosted voltage. At high Vcc values (e.g., 7 volts), the boosted voltage is then proportionately higher (e.g., 7.6 volts). This may lead to premature failure of devices receiving the boosted voltage. In other prior art arrangements, a diode is used to limit the boosted voltage. This, however, results in a transient current flow, or "spike" from the boosted node to the Vcc supply each time the boost signal is applied. This can inject noise and voltage fluctuations into the power supply and associated circuits. Also, in the case of

dynamic random access memories wherein information is stored as charge in a storage capacitor, the current spike can inject electrical carriers into the substrate that can interfere with the stored information.

The present invention is illustrated in an exemplary embodiment in FIG. 1. An input signal applied to input node 30 causes transistor M30 to conduct when node 30 is at a high voltage state. The input signal may itself be at an initially boosted level, and then return to Vcc prior to the activation of the boost capacitor, as is assumed for the exemplary case herein, in which case the conduction of M30 places the output node 38 at approximately the level of Vcc. However, the input signal can alternately be unboosted; it is then typically a threshold voltage drop below Vcc when in the high state herein. In that case, output node 38 is placed, assuming a negligible load resistance thereon, at Vcc-Vth volts.

Assuming initially that Vcc is at a relatively high level (e.g., 7 volts), no boost capacitors are activated. When the level of Vcc goes below a first threshold level, a first threshold line TH1 is activated by being placed at a high level by comparator 39. This allows NAND gate 33 to respond to the input signal, thus causing inverter 32 to bring one plate of boost capacitor 32 to a high level when the input signal is high. This in turn causes the opposite plate of C30 to boost the voltage on the output node 38. When the level of Vcc goes below a second threshold less than the first one, the comparator activates TH2 and hence, capacitor C31 in a similar manner. A third boost capacitor, C32, is likewise activated when a third threshold is reached. The present technique may be implemented using one, or more, boost capacitors up to any number.

When the input signal goes low at node 30, transistor M30 is turned off, while M31 is turned on by inverter 31. This action discharges the boosted node to a lower voltage, typically Vss, through M31. If desired,

node 38 may be discharged to a level other than Vss (0 volts), by appropriate choice of source voltage on M31. Also, when input node 30 goes low, the NAND gates 33, 35, and 37 go high, so that one plate of each of capacitors C30, C31, and C32 are brought to a low level by inverters 32, 34 and 36, respectively. This allows the boost capacitors to recharge by conduction through M31 in preparation for a subsequent boost, initiated when input node 30 again goes high.

A comparator circuit suitable for use with the present technique is shown in FIG. 2. As shown, transistors M40 and M41 serve as a voltage divider to provide a voltage at a reduced level at node 40 that is approximately comparable to the value of the switching thresholds of the inverters connected thereto. The divided voltage at node 40 also tracks changes in Vcc. The divider transistors desirably have relative long channel lengths and narrow channel widths to reduce current flow therethrough. If desired, the Vcc value applied to the drain of M40 can be derived from the output of a logic circuit that can be clocked to a high level only when the boosted voltage is desired, to further reduce power consumption. A level of about 2 volts is thus provided at node 40 in an exemplary case. The inverters comprise complementary transistor pairs M43-M44, M46-M47, and M49-M50. Optional voltage reduction transistors M42, M45, and M48 may be used to provide a reduced voltage across the inverters, to protect the n-channel transistors from "hot carrier" effects, if desired. A regulated reference voltage, Vref, is provided as shown, and has a typical value of about 5.5 volts. The three inverters have p- and n-channel transistors of differing gain ratios, to provide for different inverter switching thresholds. For example, choosing M49 and M50 to have equal gains provides a switching threshold of about one-half of the voltage across the pair. If the protective transistor M48 has a threshold of about 1.5 volts, then about 4 volts appears

across M49-M50. Hence, the switching threshold is about 2 volts. Choosing the p-channel transistor in a pair to have a larger gain than the n-channel one produces a higher (more positive) switching threshold. The differences in gain are usually produced by differences in size of the transistors; an increase in channel width, or a decrease in channel length, increase the gain.

The inverter pair M46-M47 has a higher switching threshold than M49-M50, due to M46 having a larger gain than M47, whereas inverter M43-M44 has a still higher threshold. The result is that threshold control lines TH1-TH3 activate the corresponding boost capacitors (C30-C32 in FIG. 1, respectively) as the voltage level of Vcc decreases, and deactivate them when Vcc increases, as noted above. The degree of boost is determined in part by the size of the boost capacitors in relation to the load capacitance (C33 in FIG. 1). Note that the deactivated capacitors also serve as a load to some extent, depending on the output resistances of the associated inverters. A typical relationship between the boost voltage at node 38 (V_{BOOST}) versus Vcc is shown in FIG. 3. Note that V_{BOOST} ranges only from about 6 to 7 volts when Vcc ranges from about 4 to 7 volts. Hence, a significantly improved degree of regulation of the boost is obtained as compared to prior art techniques. The foregoing discussion has shown switching thresholds that are the same whether the power supply level is increasing or decreasing. However, it is alternately possible to include a hysteresis in one or more of the thresholds. Then, a given capacitor is activated at a different (typically lower) power supply voltage than that at which it is deactivated. The hysteresis can be used to reduce the effects of noise or other disturbances that could cause "hunting" of the boosted voltage. Hence, as used herein, the term "threshold" includes the possibility of a hysteresis. However, the amount of the hysteresis for a given threshold is typically less than the difference in thresholds between

activation (or deactivation) of successive boost capacitors.

The present technique is readily implemented with typical complementary field effect transistor (e.g., CMOS) technology, but may also be implemented with bipolar transistors. Note also that while a positive boost voltage has been discussed for the illustrative case herein, a negative boost voltage is also possible. That is, voltages more negative than the reference power supply potential (Vss) are possible. In that case, the charging and discharging transistors are typically p-channel devices. The terms referring to the voltage levels associated therewith then refer to the absolute magnitude of the voltages with respect to the reference level. Note also that the above discussion has been in terms of two power supply voltages (e.g., +5 and 0 volts). However, integrated circuits are known that operate with a greater number of power supply levels. For example, emitter coupled logic (ECL) circuits operate with three voltage levels, typically 0, -2, and -5.2 volts. The boosting according to the present technique may be accomplished with respect to any of the power supply voltage levels. However, it is most typically utilized with respect to the most positive or most negative power supply voltage levels supplied to the integrated circuit.

Claims:

1. An integrated circuit comprising a node (38) adapted to being boosted to a voltage level in excess of a power supply (Vcc) level applied thereto,

CHARACTERIZED IN THAT

means are provided for boosting said node an amount dependent on said power supply level, with said means comprising a first boost capacitor (30) that is activated when said power supply level is below a first threshold, and is deactivated when said power supply level is above said first threshold, and means (39) for comparing said power supply level against said threshold.

2. The integrated circuit of claim 1 further comprising an additional boost capacitor (C31) that is activated when said power supply level is below a second threshold, and is deactivated when said power supply level is below a second threshold, and is deactivated when said power supply level is above said second threshold, wherein said second threshold is less than said first threshold.

3. The integrated circuit of claim 1 further comprising a row of memory cells each of which comprises an information storage capacitor and an access transistor connected thereto, wherein said row of memory cells is selected when a corresponding row conductor is placed at a high voltage level, and wherein said node adapted to being boosted supplies said high voltage level.

4. The integrated circuit of claim 1 further comprising a voltage comparator means for activating said boost capacitor when said power supply level is less than said first threshold, and for deactivating said boost capacitor when said power supply level is above said first threshold.

5. The integrated circuit of claim 4 wherein said voltage comparator comprises an inverter comprising a p-channel field effect transistor and an n-channel field effect transistor having a first gain ratio.

6. The integrated circuit of claim 5 wherein said

voltage comparator means further comprises a second inverter comprising a p-channel field effect transistor and an n-channel field effect transistor having a second gain ratio different from said first gain ratio.

7. The integrated circuit of claim 1 wherein said means provides a hyusteresis for said first threshold, wherein said first boost capacitor is activated at a lower power supply level than that at which it is deactivated.

FIG. 1

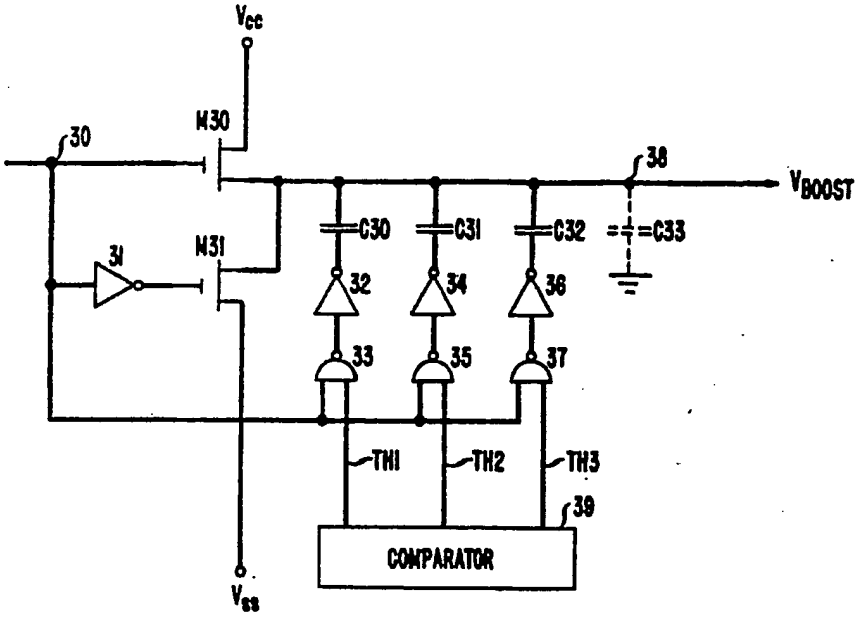


FIG. 3

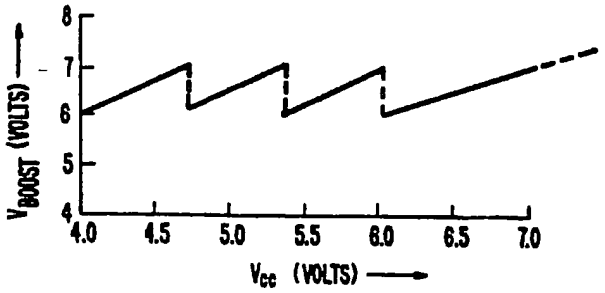
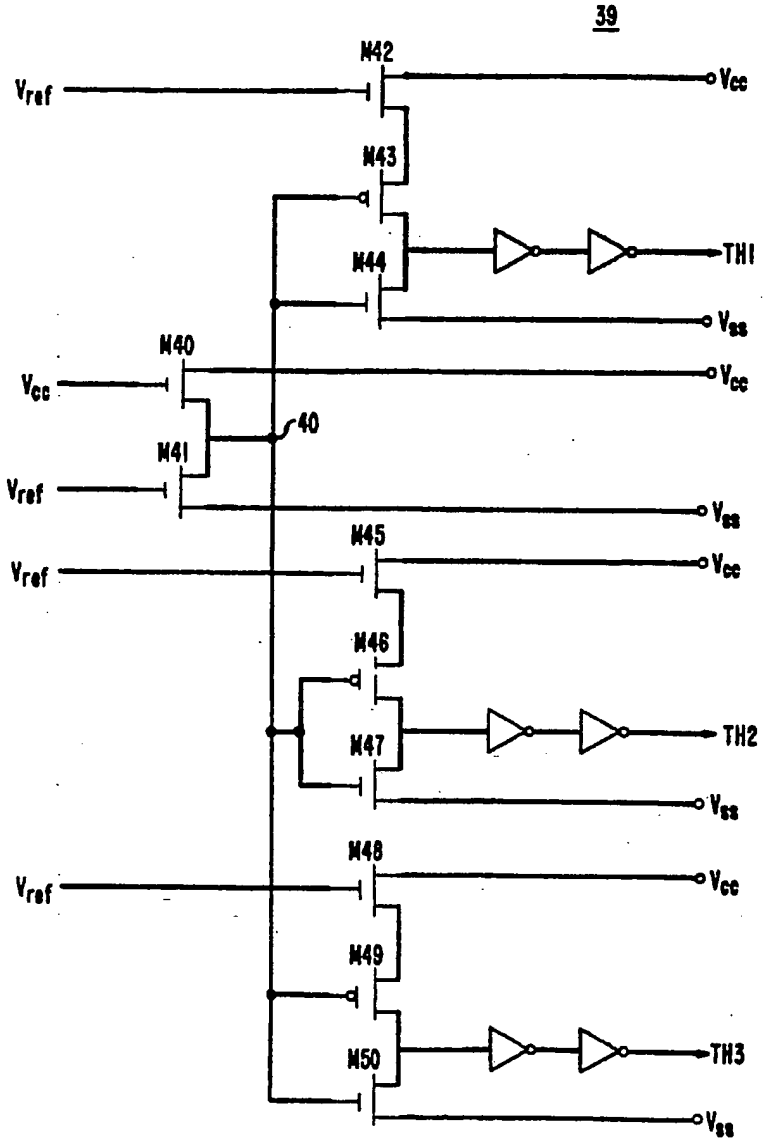


FIG. 2


39
M42
V_{ref}
V_{cc}
M43
M44
TH1
V_{ss}
M40
V_{cc}
V_{cc}
40
M41
V_{ref}
V_{ss}
M45
V_{ref}
V_{cc}
M46
M47
TH2
V_{ss}
M48
V_{ref}
V_{cc}
M49
M50
TH3
V_{ss}

INTERNATIONAL SEARCH REPORT

International Application No PCT/US 86/00160

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC[4]: G 11 C 5/00; G 05 F 5/00; G 05 F 1/62

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
IPC[4]	G 11 C; G 05 F

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category [10]	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
X	US, A, 3656052 (GENUIT et al.) 11 April 1972 see abstract; column 1, lines 70-75; column 2, lines 1-7; column 4, lines 7-75; column 5, lines 1-10; figure 1	1,4
A	--	2
Y	EP, A3, 0106222 (FURUYAMA) 25 April 1984 see abstract; page 3, lines 20-24; page 4, lines 7-37; page 5, line 1; page 7, lines 11-35; page 8, lines 1-9; lines 18-20; page 10, lines 12-28; claim 1; figures 2-5	1,4
A	--	3,5
Y	US, A, 4186329 (I.A. FAIRBAIRN) 29 January 1980 see abstract; column 1, lines 35-52; figure 1	1,4
A	-- EP, A3, 0092809 (ASANO et al.) 2 November 1982 see page 2, lines 18-22; figure 1A	3

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IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
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ANNEX TO THE INTERNATIONAL SEARCH REPORT ON

INTERNATIONAL APPLICATION NO. PCT/US 86/00160 (SA 12028)

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US-A- 3656052	11/04/72	FR-A,B 2121546	25/08/72
EP-A- 0106222	25/04/84	JP-A- 59068891	18/04/84
US-A- 4186329	29/01/80	GB-A- 1586782	25/03/81
EP-A- 0092809	02/11/83	JP-A- 58185091	28/10/83